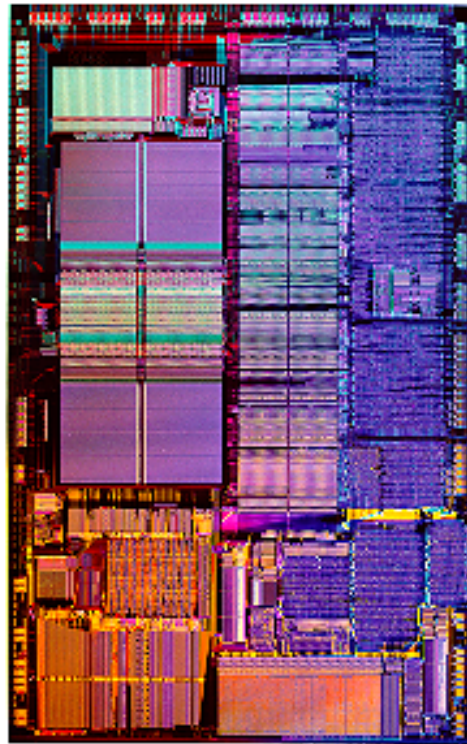
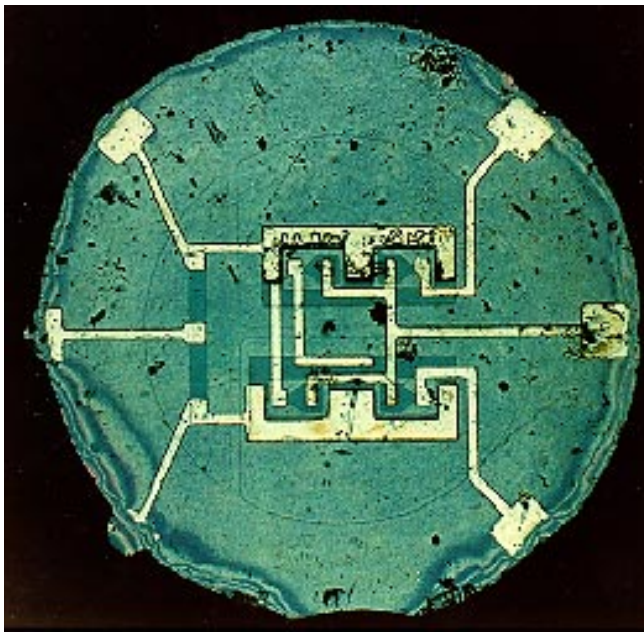


INTRODUCTION - Chapter 1 in the Text

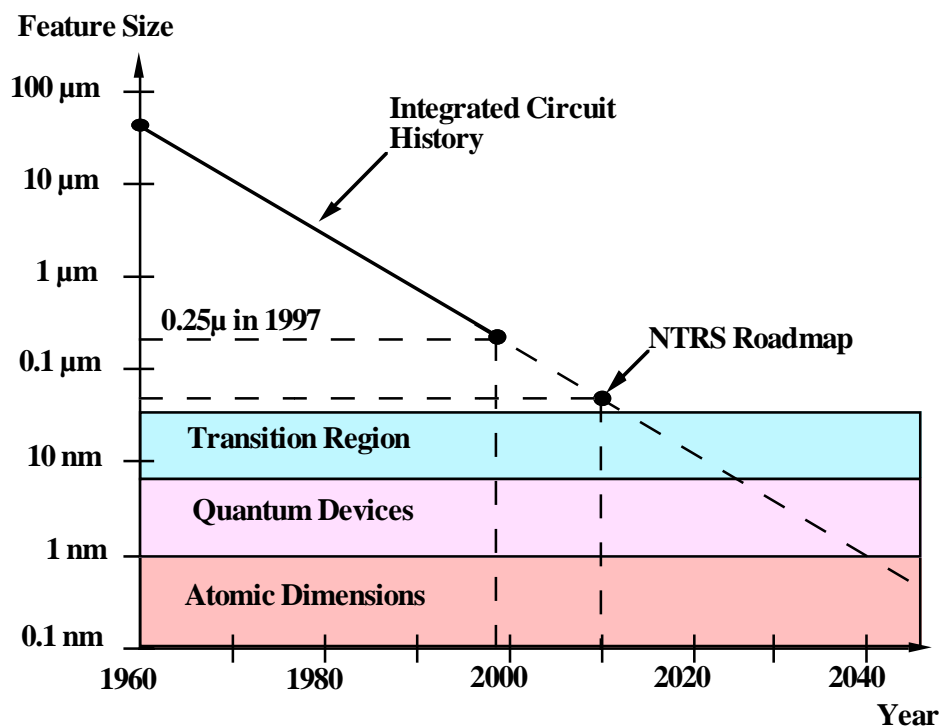
- **This course is basically about silicon chip fabrication, the technologies used to manufacture ICs.**
- **We will place a special emphasis on computer simulation tools to help understand these processes and as design tools.**
- **These simulation tools are more sophisticated in some technology areas than in others, but in all areas they have made tremendous progress in recent years.**



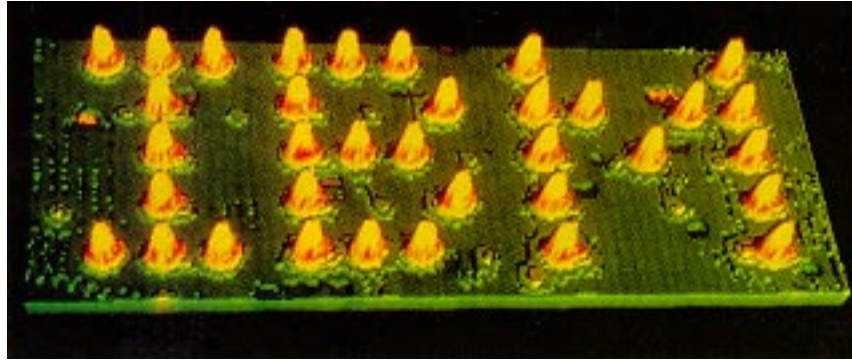
- **1960s and early 1990s integrated circuits.**
- **Progress due to:**
 - Feature size reduction - $0.7X/3$ years (Moore's Law).**
 - Increasing chip size - $\approx 16\%$ per year.**
 - “Creativity” in implementing functions.**

Year of 1st DRAM Shipment	1997	1999	2003	2006	2009	2012
Minimum Feature Size	250 nm	180 nm	130 nm	100 nm	70 nm	50 nm
DRAM Bits/Chip	256M	1G	4G	16G	64G	256G
DRAM Chip Size (mm ²)	280	400	560	790	1120	1580
Microprocessor Transistors/chip	11M	21M	76M	200M	520M	1.40B
Maximum Wiring Levels	6	6-7	7	7-8	8-9	9
Minimum Mask Count	22	22/24	24	24/26	26/28	28
Minimum Supply Voltage (volts)	1.8-2.5	1.5-1.8	1.2-1.5	0.9-1.2	0.6-0.9	0.5-0.6

- **SIA NTRS (selected data). Updated ITRS available at http://public.itrs.net/Files/1999_SIA_Roadmap/Home.htm**



- **History and future projections for minimum feature size in silicon chips.**
- **Device limits appear today to be ≈ 25 nm (250 \AA) channel lengths in MOS transistors.**

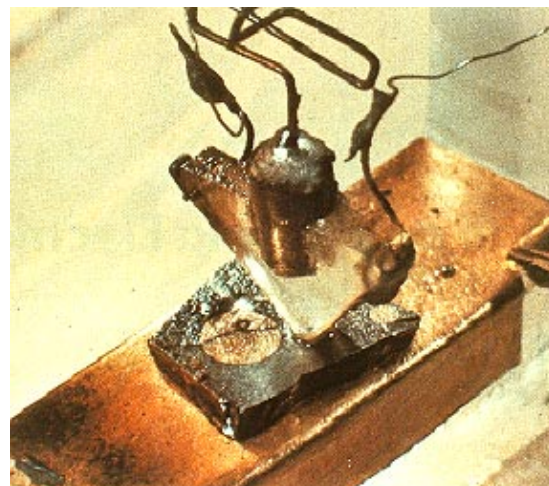
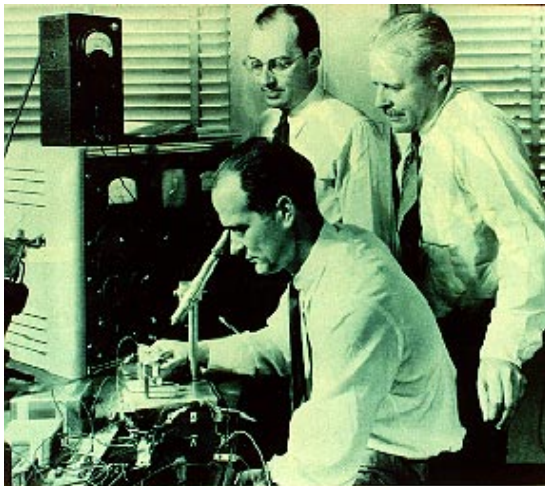


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- 1990 IBM demo of Å scale “lithography”.
- Technology appears to be capable of making structures much smaller than currently known device limits.

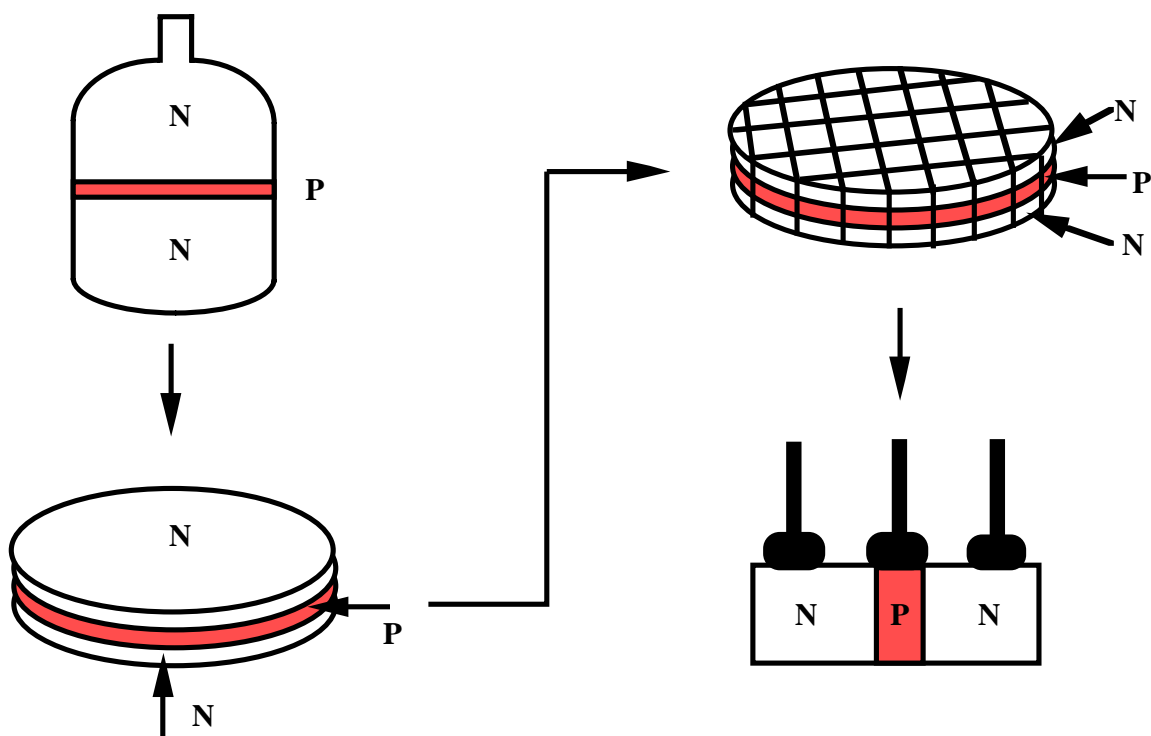
Historical Perspective

- How did we get to today’s planar technology?

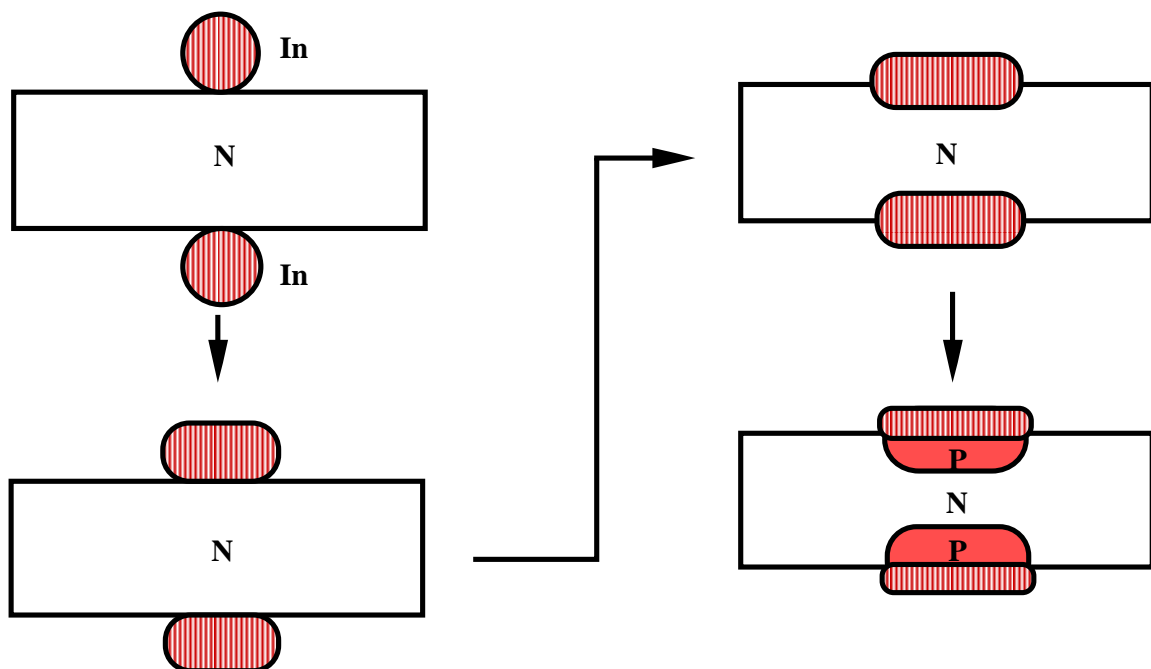


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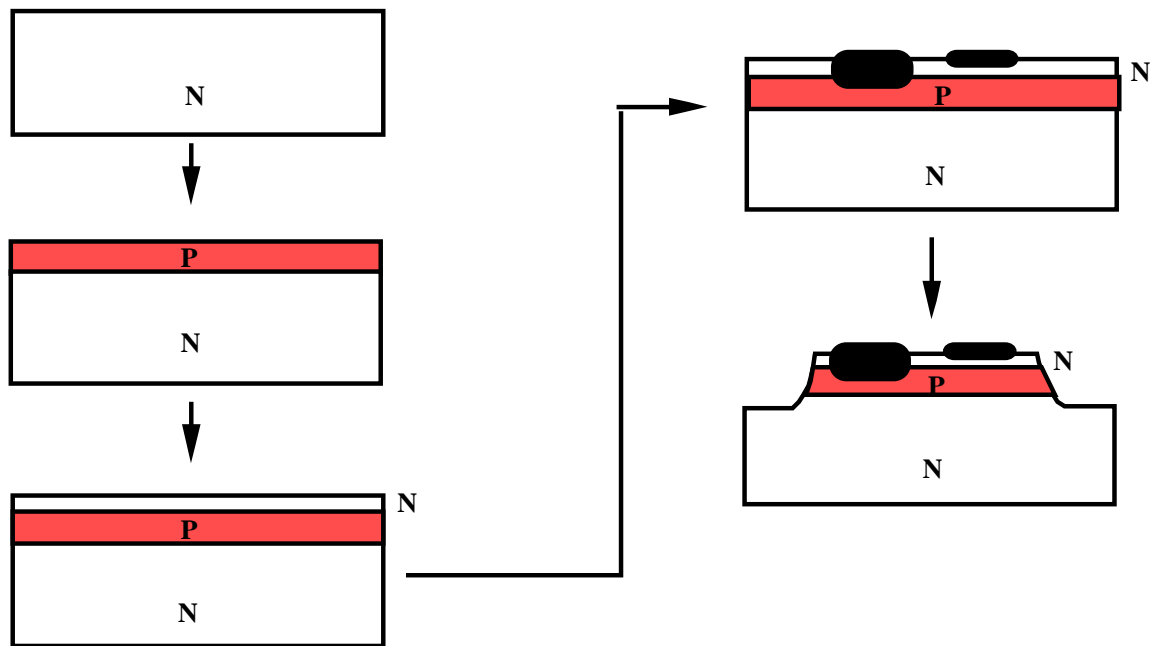
- Invention of the bipolar transistor - 1947, Bell Labs.
- Shockley’s “creative failure” methodology.



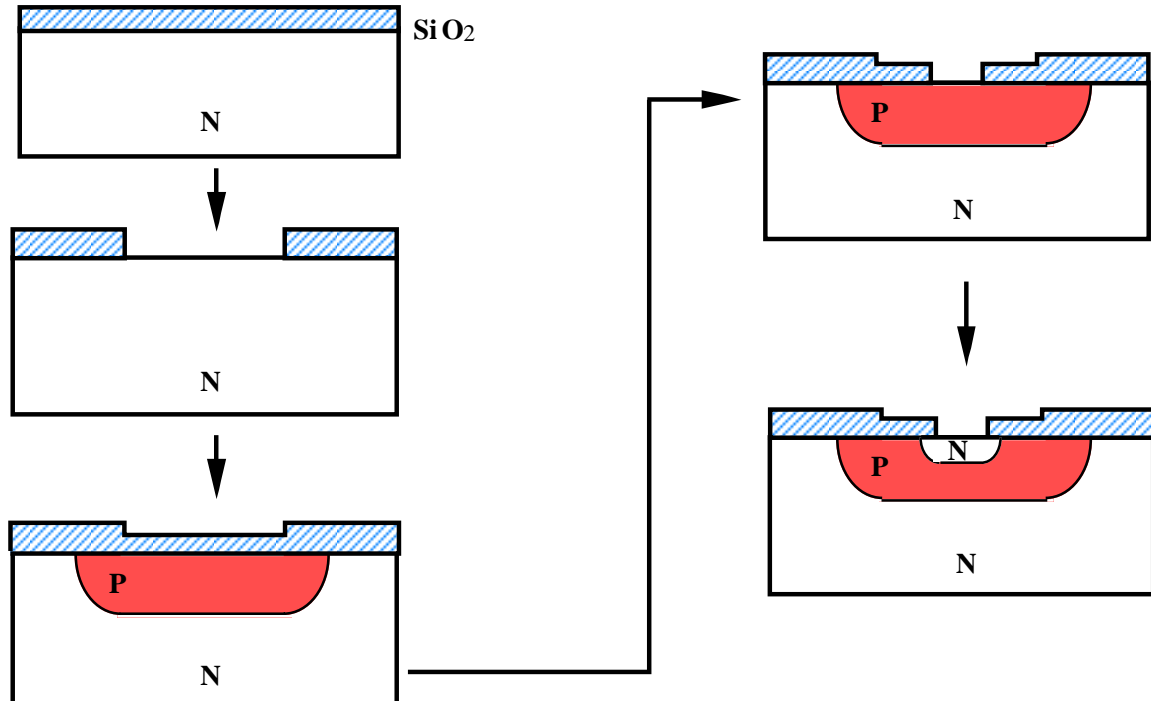
- **Grown junction transistor technology of the 1950s.**



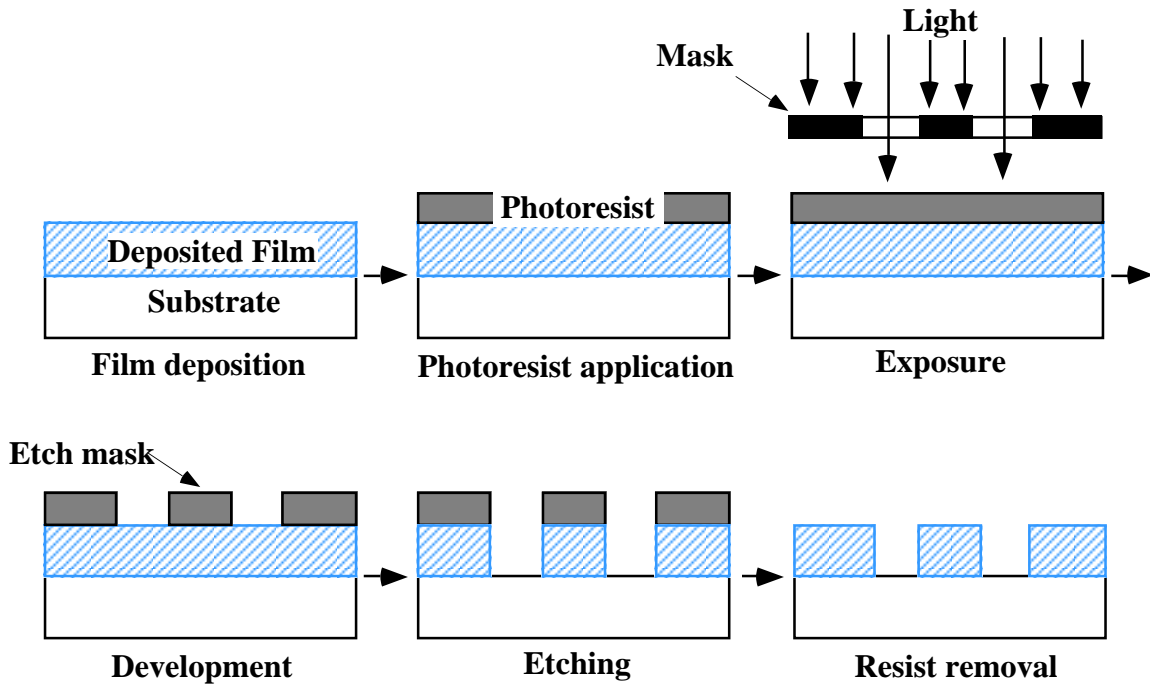
- **Alloy junction technology of the 1950s.**



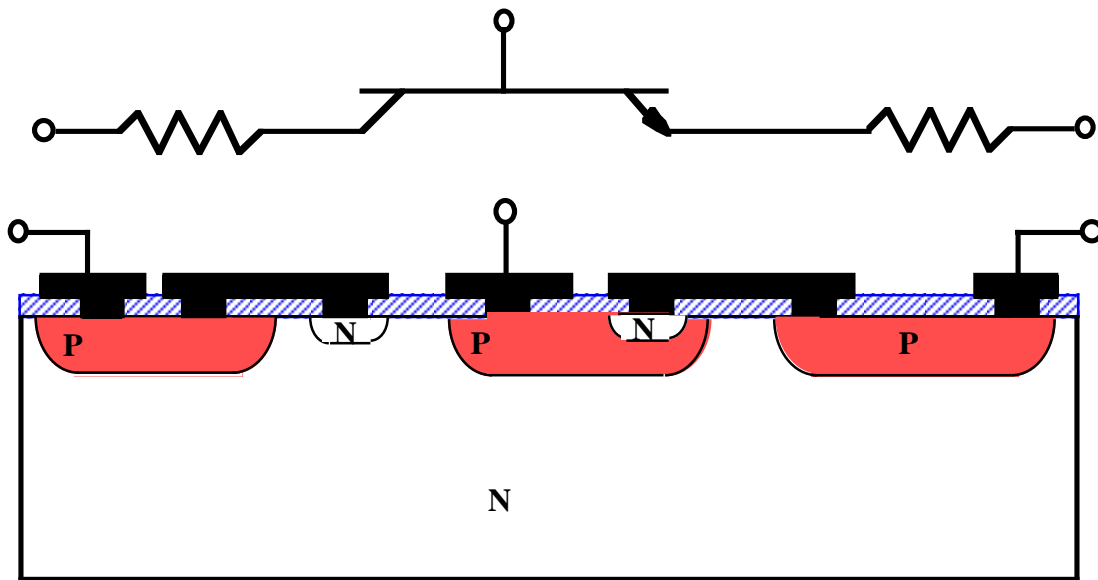
• **Double diffused transistor technology of the 1950s.**



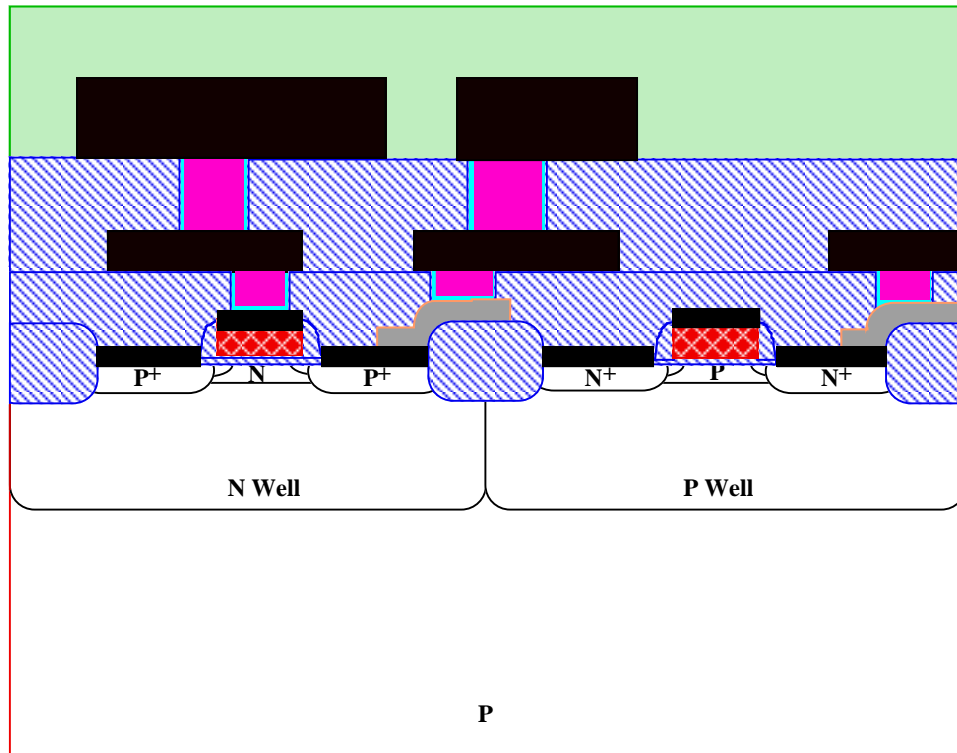
• **The planar process (Hoerni - Fairchild, late 1950s).**



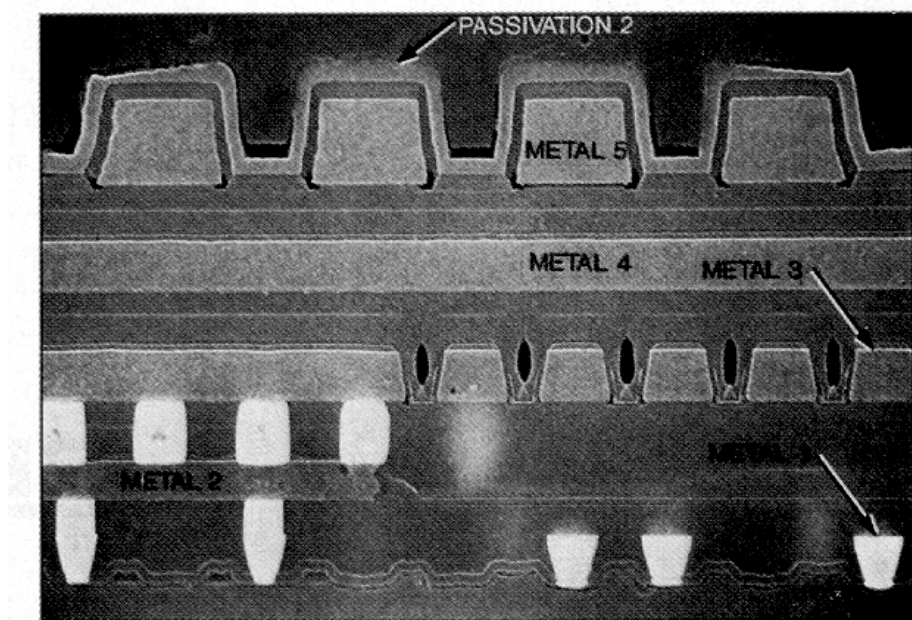
- **Basic lithography process which is central to today's chip fabrication.**



- **Lithographic process allows integration of multiple devices side by side on a wafer.**



- Schematic cross-section of a modern silicon IC.

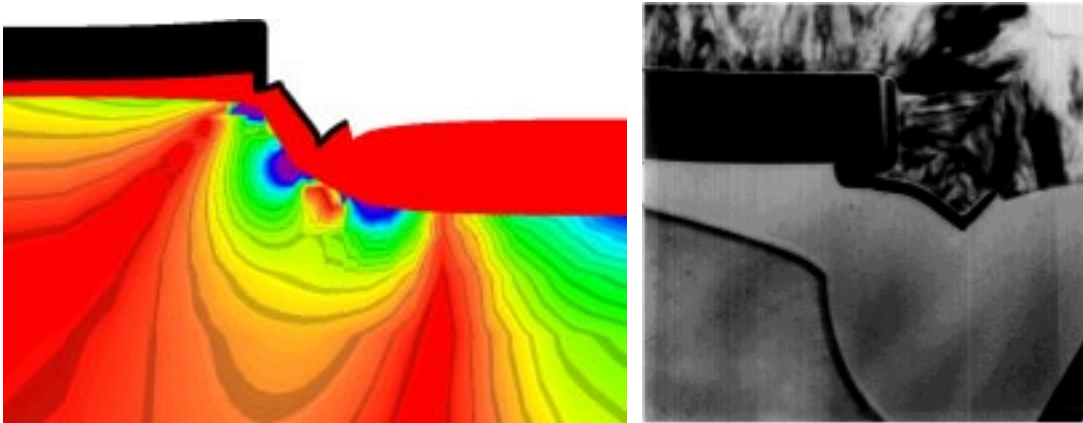


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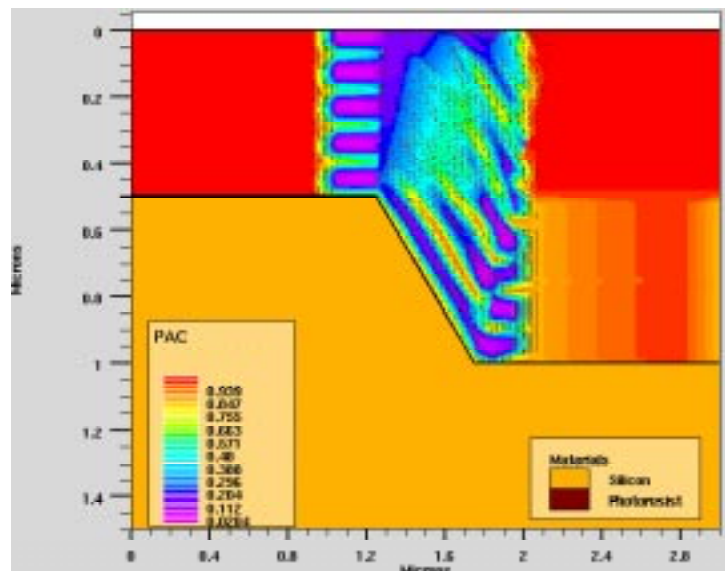
- Actual cross-section of a modern microprocessor chip.
Note the multiple levels of metal and planarization.

Computer Simulation Tools (TCAD)

- Most of the basic technologies in silicon chip manufacturing can now be simulated.
- Simulation is now used for:
 - Designing new processes and devices.
 - Exploring the limits of semiconductor devices and technology (R&D).
 - “Centering” manufacturing processes.
 - Solving manufacturing problems (what-if?)



- Simulation of an advanced local oxidation process.



- Simulation of photoresist exposure.

Summary of Key Ideas

- **ICs are widely regarded as one of the key components of the information age.**
- **Basic inventions between 1945 and 1970 laid the foundation for today's silicon industry.**
- **For more than 30 years, "Moore's Law" (a doubling of chip complexity every 2-3 years) has held true.**
- **CMOS has become the dominant circuit technology because of its low DC power consumption, high performance and flexible design options.**
- **Future projections suggest these trends will continue through at least 2010 and likely beyond.**
- **Computer simulation tools have been widely used for device, circuit and system design for many years. New tools are now being used for technology design as well.**
- **Chapter 1 also contains some review information on semiconductor materials and basic semiconductor devices for students who have not studied this material or who wish to review these areas. These topics will be useful in later chapters of the text.**